Examples of CVD Reactors and Processes

- Controlling kinetics
    - Mass transport limited at high temperatures or pressures
        - under these conditions it is important to control gas flow and pressure in order to get stable, uniform films
    - reaction rate limited at lower pressures and temperatures
        - here film growth critically depends on temperature so need a uniform temperature profile to control uniform thickness everywhere
    - reactor design differs depending on controlling mechanism
- APCVD: room pressure, fast
    - belt reactors
    - bell reactors
    - tube furnace
        - need to tilt samples to allow all samples to see the same concentration of gas
    - APCVD in general gives fast deposition rate but poor step coverage and contamination
- LPCVD: better step coverage, slower deposition rate
    - lower pressure so have reaction rate limited regime, gas flow is no longer so critical
    - better step coverage comes from less variation in arriving angles
    - stacked boat tube furnace
    - require relatively high temperatures to get significant deposition rate (due to low pressures)
    - improves step coverage and contamination issues significantly, trade off is lowered deposition rate
- PECVD: lower temperature because more energy present to initiate reaction
    - can initiate a reaction at lower temperatures (plasma acts as a catalyst)
    - still uses a low pressure so we have good step coverage and low contamination

- ***CVD of Silicon***
    - Give some examples of when you CVD silicon

        - Epi
            - Relatively thick
            - Need a great crystal structure: high temperature and/or low deposition rate to allow atoms to move around on surface and find proper add site
        - Poly gate
            - Good interface with SiO_2, resistivity, thickness
        - Structural components for surface micromachining in MEMS
            - Film stress
            - Thickness, contamination
            - Mechanical values
                - Young's modulus
                - Stiction
                - Wear, fatigue
- **Poly: Typical chemistry**: Silane (SiH_4): typically used for poly & MEMS
        - Silane is absorbed and decomposes to SiH_2 which then decomposes to Si
            - SiH_4 (g) $\rightarrow$ SiH_4 (ab)
            - SiH_4 (ab) $\rightarrow$ SiH_2 (ab) + H_2 (ab)
            - SiH_2 (ab) + H_2 (ab) $\rightarrow$ Si + H_2 (ab)
            - H_2 (ab) $\rightarrow$ H_2 (g)
        - Desorption of H_2 is believed to be slow compared to other steps, gets harder as deposition rate gets faster so rate levels off
    - Typically silane in an LPCVD (stacked boat) reactor run at 580-650°C
        - Higher temps- >750°C, get homogeneous decomposition of silane
        - Lower temperatures- too slow a deposition rate
        - Expected trends
            - Increases exponentially with temperature
            - Varies linearly with pressure (Fig. 6.28)
                - Only seen for low pressures, at higher pressures it may be due to adsorption of H_2 on surface (which suppresses the forward reaction)
    - LPCVD reactors

        - Batch
            - Example process flow:
                - 620°C, 0.2-1 Torr, silane flow rate= 250 sccm, 8-10 nm/min
                    - 2.5 hours to deposit 300 nm thick film
            - Ramp temperatures as much as 30°C to overcome effects of gas depletion
                - poly film quality, characteristics such as grain size and structure and preferred orientation, are strongly dependent on temperature and pressure
                - this means that temperature ramping across the chamber to control a uniform deposition rate will affect the grain structure!
                - Distributed feed is more common
        - Single wafer: Too slow a deposition rate to use same process as in batch LPCVD
            - Use RTCVD, temp 700°C
                - 2-3 minutes per wafer, can get similar throughput to batch

- **Epi Si**
    - Approximately 5 μm thick, need a relatively high deposition rate
        - 10 nm/min of LPCVD would take 500 min=8.3 hours
    - High temperature needed for single crystal: Fig 7.5
    - Typical chemistry: Si-H-Cl
        - SiH_xCl_{4-x}
            - Si tetrachloride ($SiCl_4$)
            - Dichlorosilane (DCS: SiH_2Cl_2)
            - trichlorosilane ($SiHCl_3$)
        - The Cl component is an advantage over silane because it reduces gas phase reactions and also cleans surface (reacts with metal impurites to form volatile gases)
        - Compare growth rates for different chemistries: *Fig 7.6*
            - The larger the Cl number, the slower the mass transport (lower D)

- At lower temperatures, process is creating polysilicon (single crystal occurs at about the knee in the graph)
- Similar slopes (similar E_A) for reaction rate indicating similar chemistries taking place
  - this is theorized to be the fact that the desorption of H_2 limits the reaction (H_2 has to leave before solid Si can form)
- SiH_4 used when low temperature deposition is needed
  - faster deposition rate at lower temperatures
  - prone to gas phase nucleation

- **CVD Reactors used for epi**
  - In order to get single crystal material, Si atoms on surface must have time to diffuse to kink and add in proper place before more Si atoms come down
    - **need slow deposition rate or high temperature**
  - Historically done in an APCVD reactor
    - Batch- barrel reactor with IR heating
      - Gas injected at top, exhausted from bottom
        - Boundary layer above wafers contributes to autodoping and doping from wafer to wafer
        - Heated from front because experimentally shown to cause less slip in wafers
    - Single wafer
      - Barrel is hard for large wafers
      - Inner chamber is made of fused quartz because stainless stell reacts with Cl at these high temperatures
  - LPCVD can be used to reduce autodoping
    - Smaller boundary layer so traps less dopant atoms (less all atoms)
- **Autodoping of Epi layers**
  - Epi layers are intentional doped as well as become doped from doped bulk Si below (autodoping)
    - significant if deposition rate $v < 2(D/t)^{1/2}$

        - otherwise, diffusion is slow relative to the depositing film
        - In that case, autodoping may arise from vaporization of dopants in the bulk Si into the gas
            - this is a transient effect: the flux from dopant in the bulk Si diminishes as the bulk material gets buried
        - Ways to reduce autodpoing
            - lower temperature
            - reduced pressure
            - low temperature purge after HCL etch to assure dopants removed during etch are swept out
            - choose dopants that have low diffusion coefficients and low vapor pressures (for example : Sb rather than As[high vapor pressure] and P[high diffusivity])
            - seal backside with lightly doped Si or silicon dioxide- so backside doesn't outgas

- **CVD of Silicon Dioxide**
    - Gate oxide is thermally grown
    - Insulation layer: low k dielectric
        - Shallow trench isolation
        - Interlayer dielectric
    - MEMS
        - sacrificial layer
        - etch barrier for bulk micromachining
    - Film characteristics
        - Uniform thickness and composition
            - Greatly impacts etch properties
- **SiO_2 with Silane chemistry**
    - Low Temperature (<500°C)
        - typically: $SiH_4 + O_2$
            - $SiH_4\,(g) + O_2\,(g) \rightarrow SiO_2 + 2H_2\,(g)$

        - SiH_4 (g)+ $2O_2$ (g)→SiO_2+$2H_2O$ (g)

- **Doped SiO2 with silane:**
  - Why add dopants?
    - P: getters contaminants (mobile alkali ions) such as Na, K, Fe, Cr, Mg...
    - B & P reduce glass transition temperature: oxide flows at a lower temperature
    - reduces stress in the films
    - increases moisture barrier of film
    - Add as much as 8 wt % P: too much and glass becomes hygroscopic (readily taking up an retaining moisture) & get corrosion problems
  - P chemistries: PSG: phosphosilicate glass
    - $SiH_4 + 6O_2 + 4PH_3 \rightarrow SiO_2 + 2P_2O_5 + 8H_2$
    - amount of P_2O_5 depends on PH_3 content
  - BPSG: borophosphosilicate
    - $SiH_4 + 5O_2 + B_2H_6 + 2PH_3 \rightarrow SiO_2 + P_2O_5 + B_2O_3 + 8H_2$ $4PH_3$ (g)+ $5O_2$ (g)→ $2P_2O_5$ (s)+$6H_2$ (g)
- **Silane deposition reactors**
  - APCVD belt reactors, distributed feed LPCVD, PECVD .
    - advantages: low temperature deposition, used after Al is deposited
    - disadvantages: poor step coverage, gas phase reactions
  - Densification Anneal: 700-1000°C anneal is sometimes done to improve density of film
    - Believed to drive out H
- **SiO_2 using TEOS Chemistry:** Intermediate temperature (700-850°C)
  - Silane is pyrophoric (ignites on contact with air!!) so often TEOS (tetraethyloxysilane: $Si(OC_2H_5)_4$) is preferred in fabs
    - $Si(OC_2H_5)_4 \rightarrow SiO_2 + 4C_2H_4 + 2H_2O$
    - Intermediate temperatures, LPCVD: temperature around 650-750°
      - At lower temperatures the deposition rate is too slow
    - PECVD at 250-425°C
  - lower temperature: with ozone

        - $Si(OC_2H_5)_4 + O_3 \rightarrow SiO_2 + 2(C_2H_5)_2O + 3/2O_2$
        - APCVD: temperature around 250-450°C
        - Gives relatively high deposition rates at low temperatures
    - advantages
        - eliminates nasty silane
        - good step coverage/ uniformity
        - comparable deposition rates
    - disadvantage
        - higher temperature
        - supplied as a liquid and put into a carrier gas using a bubbler
- **Si_3N_4**
    - DCS & ammonia (NH_3)
        - $3SiCl_2H_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2$
        - LPCVD: temperatures around 700-800°C
    - SiH_4 and NH_3
        - $3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$
        - APCVD: 700-900°C
        - lower temperature PECVD: 350-400°C
            - Deposition rate & density as a function of ammonia content, temperature, & total pressure
- W
    - Chemistries
        - $WF_6 + 3H_2 \rightarrow W(s) + 6HF$
            - also going on is: $WF_6 + 3Si(s) \rightarrow 2W(s) + 3SiF_4$ which is the basis for selective deposition
        - $2WF_6 + 3SiH_4 \rightarrow 2W(s) + 6H_2$
        - $WCl_6 + 3H_2 \rightarrow W(s) + 6HCl$
            - less common than F based chemistry because WCl_6 is a solid at room temperature and must be heated to 170°C to get reasonable vapor pressures

- PECVD
  - WF_6, around 45MHz
  - 40-90°C but not hotter: hotter creates too many F radicals which begin to etch the W
  - add H_2 to promote creation of HF radicals and achieve a higher deposition temperature